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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,927	03/16/2004	Akiyoshi Aoyagi	9319S-000669	2334

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,927	AOYAGI, AKIYOSHI	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10 and 12-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10 and 12-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed 9 February 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Taniguchi et al. (U.S. Patent 6,388,333).

In re claims 14 and 16, Taniguchi discloses a method of making a semiconductor device (Figs. 14 and 15) that contains the steps of mounting a first semiconductor chip (electronic part) (3 on the bottom) face down on a first carrier substrate (1) so that the reverse face of the first semiconductor chip (first electronic part) is exposed, mounting a second semiconductor chip (second electronic part) (3) on a second carrier substrate (1 above first chip), sealing the second semiconductor chip (second electronic part) with a sealing resin (2) and connecting the second carrier substrate to the first carrier substrate via protruding electrodes (7 between first and second carriers) so that the

second carrier substrate is held above the first semiconductor chip (first electronic part) so as to be separated from the first semiconductor chip (first electronic part).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,5 and 12-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi in view of Yamamoto (JP 2001-110979).

In re claims 1,12 and 13, Taniguchi discloses a semiconductor device (Figs. 14 and 15) that contains a first carrier substrate (1), a first semiconductor chip (first electronic part) (3 above 1) having a mounting face and a reverse face on an opposite side of the first semiconductor chip from the mounting face, the first semiconductor chip being mounted face down on the first carrier substrate such that the mounting face opposes the first substrate, a second carrier substrate (1 above first chip), a second semiconductor chip (second electronic part) (3) mounted on the second carrier substrate, protruding electrodes for connecting the second carrier substrate to the first carrier substrate so the second carrier substrate is held above and spaced apart from the first semiconductor chip such that a gap is created between the first semiconductor chip and the second carrier substrate, exposing the reverse face of the first semiconductor chip and a sealant (2) sealing the second semiconductor chip.

Taniguchi discloses all the limitations except for a resin provided between the first and second carriers where the reverse face of the chip (electronic part) is exposed. Whereas Yamamoto discloses a semiconductor device (Fig. 1) that contains a first carrier substrate (20) and second carrier (15) with a first semiconductor chip (19) mounted on first carrier substrate with a resin provided between the first and second carrier substrate so the reverse face of the first semiconductor chip is exposed. The resin is formed on the first semiconductor chip to seal and encapsulate the first semiconductor chip. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Taniguchi by incorporating a resin between the first and second carrier substrate to encapsulate and seal the first semiconductor chip as taught by Yamamoto.

In re claim 2, Taniguchi discloses the second carrier substrate is fixed to the first carrier substrate so as to be mounted on the first semiconductor chip. (Fig. 15)

In re claim 3, Taniguchi discloses the sealant further comprises a mold resin. (Column 8, line 42)

In re claim 5, Taniguchi discloses all the limitations except for the first semiconductor chip connected to the first carrier substrate by pressure welding. This limitation is a process limitation. A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final

product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear. Even though product –by [-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted)."

Claims 4 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi and Yamamoto as applied to claim 1 above, and further in view of Nishimura et al. (U.S. Patent 6,781,241).

In re claims 7-10, Taniguchi and Yamamoto disclose all the limitations except for a plurality of first and second semiconductor chips. Whereas Nishimura discloses a semiconductor device (Fig. 6) that contains a plurality of first semiconductor chips (3a/b) that are flip chip mounted ball grid arrays and are mounted parallel on the first carrier substrate (1b) and a plurality of stacked second semiconductor chips (3c/d) that are ball grid array and chip size package formed on a second carrier substrate (1a). There is a plurality of first and second semiconductor chips to allow for heat transfer to the first and second carrier substrates. (Column 7, lines 35-44) Therefore it would have been

obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Taniguchi and Yamamoto by incorporating a plurality of first and second semiconductor chips to allow heat transfer from the chips to the first and second carrier substrates as taught by Nishimura.

In re claim 4, Nishimura discloses the sidewall of the sealant (2) coincides with a sidewall of the second carrier substrate. (Fig. 6)

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi in view of Wachtler (U.S. Publication 20030022465).

In re claim 15, Taniguchi discloses all the limitations except for the second chips molded and cut. Whereas Wachtler discloses wafer package (Figs. 16 and 17) that contains semiconductor chips (204) integrally molded on a carrier substrate (134) with a sealing resin where the carrier substrate is cut with the sealing resin so each piece includes one semiconductor chip. The carrier substrate is cut so as to produce individual molded chip for integrated circuit packages. (Page 6, Paragraph 62) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Taniguchi by incorporating cutting the carrier with the molded semiconductor chip to produce individual molded chip for integrated circuit packages as taught by Wachtler.

Response to Arguments

Applicant's arguments with respect to claims 1-5,7-10 and 12-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

Zandra V. Smith
Supervisory Patent Examiner
12 May 2006